CLAIMS

1. (Currently Amended) A method of varying the loop bandwidth of a PLL (Phase Lock Loop), comprising the steps of:

inserting a switched capacitance in ~~the~~ a damping resistor leg of a low pass filter portion of the PLL; ~~and~~

switching the switched capacitance, as a function of a reference frequency and ~~the~~ a divided PLL output frequency [[.]] wherein said function is a substantially continuous difference between the reference frequency and the divided PLL output frequency.

2. (Currently Amended) The method of claim 1, wherein [[~~:~~]] said switched capacitance is connected in parallel with a damping resistor. ~~; and~~

~~said function is the difference between the reference frequency and the PLL output frequency.~~

3. (Original) The method of claim 2, comprising the additional steps of:

mixing said reference frequency and said PLL output frequency to generate a difference frequency; and

applying said difference frequency to said switched capacitor to alternately connect said switched capacitor to opposite ends of said damping resistor.

4. (Currently Amended) A method of varying the loop bandwidth of a PLL (Phase Lock Loop), comprising the steps of:

generating a switching signal that is a function of a reference frequency and ~~the~~ a divided PLL output frequency, wherein said function is a substantially continuous difference between the reference frequency and the divided PLL output frequency;

inserting a switchable capacitor in a damping resistor leg of a low pass filter portion of the PLL; and

varying the effective impedance of the damping resistor leg by switching the connections of said switchable capacitor in accordance with said switching signal.

5. (Currently Amended) A PLL (Phase Lock Loop), comprising:

a PFD (Phase Frequency Detector) including first and second inputs and an output;

a reference signal of frequency F1 connected to said first input of said PFD;

a VCO (Voltage Controlled Oscillator) including an input and an output providing an output signal of frequency F2 when the PLL is in a stable condition;

a signal frequency divider, operable to alter the frequency of the VCO output signal by a ratio of F1/F2, connected between said output of said VCO and said second input of said PFD;

a mixer connected to said first and second inputs of said PFD, said mixer providing a variable frequency output signal F3 indicative of the difference in frequency of the first input and the second input ~~two signals~~ received by said PFD;

an LPF (Low Pass Filter) connected between said output of said PFD and said input of said VCO and further connected to receive the signal F3 from said output of said mixer; and

a variable impedance damping resistor ~~comprising a~~ which is part of said LPF, the impedance of said variable impedance damping resistor being a function of the frequency of the signal F3.

6. (Currently Amended) The apparatus of claim 5, wherein:

said variable impedance damping resistor comprises a switched capacitor circuit; and

the impedance of said damping resistor increases ~~and~~ as the frequency of the signal F3 decreases.

7. (Currently Amended) A PLL (Phase Lock Loop), comprising:

a PFD (Phase Frequency Detector);

a VCO (Voltage Controlled Oscillator);

a signal frequency divider, operable on ~~to alter~~ the frequency of the VCO output signal by a ratio of F1/F2 where F1 is the frequency of a reference signal used by said PLL and F2 is the desired output frequency of the PLL when in a stable condition; and

an LPF (Low Pass Filter) connected between an output of said PFD and an input of said VCO, said LPF including a variable impedance damping resistor, the impedance of said variable impedance damping resistor varying as a function of a difference between F1 [[-]] and ~~F2~~ a signal frequency divider output.

8. (Currently Amended) Apparatus for use in adaptive control of loop bandwidth in a PLL (Phase Locked Loop) system, comprising:

a PFD (Phase Frequency Detector) means having

a reference clock input having a corresponding W2 frequency component signal,

a feedback clock signal having a corresponding W1 frequency component signal, and

an output signal;

an LPF(Low Pass Filter) interconnected to said output signal, said LPF including

a switched capacitor circuit with a control input; [[,]] and

~~a W1 frequency component signal; and~~

a difference means for developing a control signal corresponding to ~~the~~ a substantially continuous difference between said W2 and W1 frequency component signals, said control signal being delivered to said control input of said switched capacitor circuit.

9. (Currently Amended) A PLL (Phase Lock Loop), comprising:

a PFD (Phase Frequency Detector) including reference first and feedback clock second inputs and an output;

a VCO (Voltage Controlled Oscillator) including an input and an output providing an output signal of a given frequency when the PLL is in a stable condition;

feedback clock means, operable to provide a feedback clock signal, connected between said output of said VCO and said second input of said PFD;

control signal supplying means, connected to said first and second inputs of said PFD, said control signal supplying means providing a control signal F1 indicative of ~~the~~ a difference between the reference clock input and the feedback clock input ~~in frequency of the two signals received by said PFD~~;

an LPF (Low Pass Filter) connected between said output of said PFD and said input of said VCO and further connected to receive the control signal F1 from ~~said~~ an output of ~~said~~ a mixer; and

a variable impedance damping resistor ~~comprising a~~ which is part of said LPF, the impedance of said variable impedance damping resistor being a function of the control signal F1.